UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,010	03/17/2004	Tae-sun Chung	Q78750	3316

23373 7590 06/11/2009
SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

MAIL DATE	DELIVERY MODE
06/11/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,010	CHUNG ET AL.	
	Examiner	Art Unit	
	JARED I. RUTZ	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-15 and 17-21* is/are rejected.

7)☒ Claim(s) *7,16 and 22-25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25, as amended on 3/6/2009, are pending in the instant application. Applicant's arguments submitted 3/6/2009 have been carefully and fully considered, but are not found persuasive. The instant Office action is made **FINAL**.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-4, 11-14, and 18- 21** are rejected under 35 U.S.C. 102(b) as being anticipated by Conley (US 2002/0099904).

3. **Claim 1** is taught by Conley as:

a. *A flash memory access apparatus, comprising: a flash memory comprising a plurality of units, each of the units comprising a plurality of blocks, and a flash memory controller.* Paragraph 0038 teaches the architecture of a typical non-volatile data storage system, which includes a controller and a plurality of flash memory devices. Paragraph 0040 explains that flash memory cells are divided into multiple pages.

b. *Wherein if a write operation is requested for a logical block number of the flash memory, the flash memory controller is configured to write data and meta-information comprising flash memory state information comprising an indicator which indicates a state of the physical block as valid, deleted, or invalid in the physical block corresponding to a logical block with the logical block number if a previous write operation has not been performed for the logical block.* Paragraph 0062 discusses a method of programming a non-volatile memory. If there are pages in the physical block that have not been written to, the data is written to those blocks. Paragraph 0055 shows a page contains a time stamp 43. Paragraph 0050 shows that the time stamp indicates the time the page was written relative to other pages with the same logical address. As shown in paragraph 0052, the time stamps of blocks having the same logical block address and page offset are compared, which allows the system to determine which page is the last written page. Accordingly, this shows what pages are valid and which pages are invalid. Additionally, when the block is erased, the timestamp field will contain all 1's, indicating that the block is deleted.

c. *And the flash memory controller is configured to perform a write operation for writing the data and the meta-information, comprising writing the valid indicator, allocated to the logical block in a new physical block without changing flash memory state information, wherein the flash memory state information is written in a previous physical block corresponding to the logical block if the previous write operation has been performed for the logical block.* Paragraph

0049 shows that when new data is to be written to a logical block corresponding to physical block PBN 0, item 35 of figure 8, which is full, a new physical block PBN 1, item 39 of figure 8, is selected and the new pages are written to PBN 1. Figure 8 also shows that original block PBN0 contains timestamps 43 and LBN and page tag 41 for each page in the original block. Paragraph 0055 shows that an individual page contains data, item 45 of figure 10, and meta-information, item 49 of figure 10. Paragraph 0048 shows that when new pages are written to a logical block, the pages containing the original data are not tagged. The last sentence of paragraph 0047 further emphasizes this by stating "*the writing of the old/new or other flags, as described with respect to FIGS. 6, 7A and 7B, cannot be tolerated.*"

d. *And wherein the flash memory state information is time independent.* Paragraph 0051 shows that the output of a modulo-N counter can be used to generate the value of field 43, which is shown in paragraph 0052 to be used to determine if a block is the most recent block.

4. **Claim 2** is taught by Conley as:

e. *The apparatus as claimed in claim 1, wherein each physical block comprises: a first area, into which the data is written, and a second area, into which meta-information is written.* Figure 10 shows that a page includes user data area 45 and overhead area 49.

5. **Claim 3** is taught by Conley as:

f. *The apparatus as claimed in claim 1, wherein data and meta-information of the logical block are simultaneously written.* Paragraph 0055 shows that the data 45 and meta-information 49 are part of the same page. As the data and meta-information are part of the same page they would inherently be written simultaneously, as the system of Conley writes data on a page basis.

6. **Claim 4** is taught by Conley as:

g. *The apparatus as claimed in claim 1, wherein the meta-information further comprises the logical block number.* Paragraph 0055 shows that overhead data, item 49 of figure 10, contains the logical block number.

h. *And the flash memory state information indicating a state of the physical block as valid, deleted, or invalid.* Paragraph 0055 shows a page contains a time stamp 43, paragraph 0051 shows that the timestamp can be replaced with the output of a modulo-N counter. Paragraph 0050 shows that the time stamp indicates the time the page was written relative to other pages with the same logical address. As shown in paragraph 0052, the time stamps of blocks having the same logical block address and page offset are compared, which allows the system to determine which page is the last written page. Accordingly, this shows what pages are valid.

7. **Claim 11** is taught by Conley as:

i. *A flash memory access method, comprising: accessing the flash memory and searching for a currently writable physical block if a processor requests a write operation for a specific logical block number of the flash memory.* Paragraph 0062 shows that when a write is performed, an available physical page is found.

j. *And writing data and meta-information, comprising flash memory state information comprising an indicator which indicates a state of the physical block as valid, deleted, or invalid, in the physical block corresponding to a logical block with the logical block number if a previous write operation has not been performed for the logical block.* Paragraph 0062 discusses a method of programming a non-volatile memory. If there are pages in the physical block that have not been written to, the data is written to those blocks. Paragraph 0055 shows a page contains a time stamp 43. Paragraph 0050 shows that the time stamp indicates the time the page was written relative to other pages with the same logical address. As shown in paragraph 0052, the time stamps of blocks having the same logical block address and page offset are compared, which allows the system to determine which page is the last written page. Accordingly, this shows what pages are valid and which pages are invalid. Additionally, when the block is erased, the timestamp field will contain all 1's, indicating that the block is deleted.

k. *And writing the data and the meta-information comprising writing the valid indicator in a new physical block corresponding to the logical block without*

changing flash memory state information, wherein the flash memory state information is written in a previous physical block corresponding to the logical block if the previous write operation has been performed for the logical block. Paragraph 0049 shows that when new data is to be written to a logical block corresponding to physical block PBN 0, item 35 of figure 8, which is full, a new physical block PBN 1, item 39 of figure 8, is selected and the new pages are written to PBN 1. Figure 8 also shows that original block PBN0 contains timestamps 43 and LBN and page tag 41 for each page in the original block. Paragraph 0055 shows that an individual page contains data, item 45 of figure 10, and meta-information, item 49 of figure 10. Paragraph 0048 shows that when new pages are written to a logical block, the pages containing the original data are not tagged. The last sentence of paragraph 0047 further emphasizes this by stating "*the writing of the old/new or other flags, as described with respect to FIGS. 6, 7A and 7B, cannot be tolerated.*"

l. *Wherein the flash memory state information is time independent.* Paragraph 0051 shows that the output of a modulo-N counter can be used to generate the value of field 43, which is shown in paragraph 0052 to be used to determine if a block is the most recent block.

8. **Claim 12** is taught by Conley as:

m. *The method as claimed in claim 11, wherein each physical block comprises first and second areas, the method further comprising: writing data*

into the first area, and writing the meta-information into the second area. Figure 10 shows that a page includes user data area 45 and overhead area 49, and paragraph 0055 shows that the corresponding data is written to each area.

9. **Claim 13** is taught by Conley as:

n. *The apparatus as claimed in claim 11, wherein the data and meta-information of the logical block are simultaneously written.* Paragraph 0055 shows that the data 45 and meta-information 49 are part of the same page. As the data and meta-information are part of the same page they would inherently be written simultaneously, as the system of Conley writes data on a page basis.

10. **Claim 14** is taught by Conley as:

o. *The method as claimed in claim 11, wherein the meta-information comprises the logical block number.* Paragraph 0055 shows that overhead data, item 49 of figure 10, contains the logical block number.

p. *And the flash memory state information indicating a state of the physical block as valid, deleted, or invalid.* Paragraph 0055 shows a page contains a time stamp, paragraph 0051 shows that the timestamp can be replaced with the output of a modulo-N counter. Paragraph 0050 shows that the time stamp indicates the time the page was written relative to other pages with the same logical address. As shown in paragraph 0052, the time stamps of blocks having the same logical block address and page offset are compared, which allows the

system to determine which page is the last written page. Accordingly, this shows what pages are valid.

11. **Claim 18** is taught by Conley as:

q. *A flash memory access apparatus, comprising: a flash memory comprising a plurality of physical blocks*. Paragraph 0038 teaches the architecture of a typical non-volatile data storage system, which includes a controller and a plurality of flash memory devices. Paragraph 0040 explains that flash memory cells are divided into multiple pages.

r. *Wherein each physical block of the plurality of physical blocks comprises data and meta-information, and the meta-information comprises a logical block number and flash memory state information*. Paragraph 0055 shows that each page contains an overhead data area 49, which includes the LBN and page tag 41 and time stamp 43, which is used to determine if the stored data is the valid data for the corresponding logical page. Figure 8 shows that original block PBN0 contains timestamp 43 and LBN and page tag 41 for each page in the original block.

s. *Wherein the flash memory state information is time independent and comprises an indicator which indicates a state of the physical block as valid, deleted, or invalid*. Paragraph 0051 shows that instead of a timestamp, a modulo-N counter may be used which is incremented each time a logical block is updated. Paragraph 0055 shows a page contains a time stamp 43. Paragraph

0050 shows that the time stamp indicates the time the page was written relative to other pages with the same logical address. As shown in paragraph 0052, the time stamps of blocks having the same logical block address and page offset are compared, which allows the system to determine which page is the last written page. Accordingly, this shows what pages are valid and which pages are invalid. Additionally, when the block is erased, the timestamp field will contain all 1's, indicating that the block is deleted.

t. *And a flash memory controller, wherein if a write operation is requested for the logical block number, the flash memory controller performs one of (a) a first write operation which writes the data and the meta-information in a first physical block corresponding to the logical block number, if the first write operation has not previously been performed for the logical block number, and changes the flash memory state information of the physical block corresponding to the logical block number.* Paragraph 0055 shows that each page contains overhead data 49. It is inherent that this data is written to the page when the first write is performed for the logical page number, as otherwise the system would be unable to tell if later written data is later or earlier.

u. *And (b) a second write operation which writes the data and the meta-information in a second physical block, if the first write operation has been performed for the logical block with the logical block number, wherein the flash memory state information of the physical block corresponding to the logical block number is not changed.* Paragraph 0049 shows that when new data is to be

written to a logical block corresponding to physical block PBN 0, item 35 of figure 8, which is full, a new physical block PBN 1, item 39 of figure 8, is selected and the new pages are written to PBN 1. Paragraph 0055 shows that an individual page contains data, item 45 of figure 10, and meta-information, item 49 of figure 10. Paragraph 0048 shows that when new pages are written to a logical block, the pages containing the original data are not tagged. The last sentence of paragraph 0047 further emphasizes this by stating "*the writing of the old/new or other flags, as described with respect to FIGS. 6, 7A and 7B, cannot be tolerated.*"

v. Additionally, the Examiner respectfully notes that that claim 18 only requires performing one of the first write operation and second operation.

12. **Claim 19** is taught by Conley as:

w. *The apparatus as claimed in claim 18, wherein each physical block comprises a main area which stores the data and a spare area which stores the meta-information, the logical block number and the flash memory state information.* Figure 10 shows that each page contains user data area 45 and overhead area 49, which includes the LBN 41 and timestamp 43.

13. **Claim 20** is taught by Conley as:

x. *The apparatus as claimed in claim 18, wherein each physical block comprises a main area into which the data is written and a spare area into which*

the meta-information is written. Figure 10 shows that each page contains user data area 45 and overhead area 49, which includes the LBN 41 and timestamp 43.

14. **Claim 21** is taught by Conley as:

y. *The apparatus as claimed in claim 19, wherein the meta-information is written in the spare area simultaneously as the data of the logical block is written in the main area*. Paragraph 0055 shows that the data 45 and meta-information 49 are part of the same page. As the data and meta-information are part of the same page they would inherently be written simultaneously, as the system of Conley writes data on a page basis.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. **Claims 5-6, 8-10, 15, and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Conley (cited *supra*) in view of Kim et al. (US 6,381, 176).

17. **Claim 5** is taught by Conley as shown *supra* with respect to claim 1.

18. Although Conley teaches that blocks having the same logical block number can be distinguished by their timestamps, it does not disclose expressly performing a recovery operation.

19. With respect to claim 5, Kim teaches:

z. *The apparatus as claimed in claim 1, wherein the flash memory controller is configured to perform a recovery operation which detects, during a scanning process, physical blocks for the logical block number and recovers from an error by determining a valid block for the logical block among the detected physical blocks*. Kim teaches at column 6 lines 29-36 that a recovery operation is required if two valid blocks having the same logical block number exist. In the system disclosed by Conley, paragraph 0050 shows that it can be determined which of multiple pages having the same logical block number and page offset is the correct page by comparing the timestamps of the blocks.

20. At the time of the invention it would have been obvious to one of ordinary skill in the art that a recovery operation is necessary in the event of an error during writing.

21. Conley and Kim are analogous art because they are from the same field of endeavor, the design of flash memory systems.

22. The motivation for doing so would have been to determine which block will be erased during a recovery operation (Kim, column 6 lines 30-36)

23. Therefore, it would have been obvious to combine Kim with Conley for the benefit of determining which pages are old and can be deleted to obtain the invention as specified in **claims 5, 6, and 8-10**.

24. **Claim 6** is taught by Conley as:

aa. *The apparatus as claimed in claim 5, wherein the scanning process comprises reading a logical block number for each of the physical blocks by investigating the flash memory based on a latest accessed block.* Paragraph 0052 shows that when the controller reads the data, it compares the counts in fields 43 and 43' of pages having the same LBA and page offset.

bb. *And investigating a field of a block allocation table corresponding to the read logical block number.* Figure 9, discussed in paragraph 0049, which is formed from the data in fields 41 and 41', shows the table that provides a mapping from logical blocks to physical blocks.

25. **Claim 8** is taught by Conley as:

cc. *The apparatus as claimed in claim 5, wherein the recovery operation recovers from an error by determining a latest accessed physical block for the logical block number among the detected physical blocks according to priorities set during the scanning process, as the valid block.* Conley paragraph 0050 shows that the most recently written page is determined by checking field 43, the timestamp.

dd. *And rewriting flash memory state information written in other physical blocks of the detected physical blocks as deleted.* Paragraph 0062 shows that updating one or more blocks of data will result in one or more blocks storing the

data to be superceded by the new data, and the blocks with superceded data are identified for erasure.

26. **Claim 9** is taught by Conley and Kim as:

ee. *The apparatus as claimed in claim 5, wherein the recovery operation is performed during the initializing the flash memory.* Kim column 4 lines 22-25 shows that when a flash memory is initially used, a logical unit number to physical unit number table is provided. To generate such a table in a system using the timestamps of Conley, it would be necessary to determine which of the pages sharing the same logical block number and page offset is the most recent page.

27. **Claim 10** is taught by Kim as:

ff. *The apparatus as claimed in claim 5, wherein the recovering from the error is performed during reclaiming the flash memory wherein the reclaiming comprises moving data written in a predetermined unit of the flash memory to a new unit.* Column 8 line 55 to column 9 line 4 teaches that in a reclaim operation, valid blocks and related metadata are copied to a new unit. In order to determine which blocks are valid in a system using the timestamps of Conley, the timestamps of pages having the same logical block number and page offset must be compared.

28. **Claim 15** is taught by Conley as shown *supra* with respect to claim 11.

29. Although Conley teaches that blocks having the same logical block number can be distinguished by their timestamps, it does not disclose expressly performing a recovery operation.

30. With respect to claim 15, Kim teaches:

gg. *The method as claimed in claim 11, further comprising a recovery operation comprising detecting, during a scanning process, physical blocks for the logical block number and of recovering from an error by determining a valid block for the logical block among the detected physical blocks.* Kim teaches at column 6 lines 29-36 that a recovery operation is required if two valid blocks having the same logical block number exist. In the system disclosed by Conley, paragraph 0050 shows that it can be determined which of multiple pages having the same logical block number and page offset is the correct page by comparing the timestamps of the blocks.

31. At the time of the invention it would have been obvious to one of ordinary skill in the art that a recovery operation is necessary in the event of an error during writing.

32. Conley and Kim are analogous art because they are from the same field of endeavor, the design of flash memory systems.

33. The motivation for doing so would have been to determine which block will be erased during a recovery operation (Kim, column 6 lines 30-36)

34. Therefore, it would have been obvious to combine Kim with Conley for the benefit of determining which pages are old and can be deleted to obtain the invention as specified in **claims 15 and 17**.

35. **Claim 17** is taught by Conley and Kim as:

hh. *The method as claimed in claim 15, wherein the recovering comprises recovering from the error by determining a latest data written among data of a specific logical block number detected during reclaiming the flash memory and wherein the reclaiming comprises moving data written in a predetermined unit of the flash memory to a new unit.* Conley paragraph 0050 shows that the most recently written page is determined by checking field 43, the timestamp. Kim column 8 line 55 to column 9 line 4 teaches that in a reclaim operation, valid blocks and related metadata are copied to a new unit. In order to determine which blocks are valid in a system using the timestamps of Conley, the timestamps of pages having the same logical block number and page offset must be compared.

Allowable Subject Matter

36. **Claims 7, 16, and 22-25** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

37. Applicant's arguments filed 3/6/2009 have been fully considered but they are not persuasive.

38. **First point of Argument**

39. In the eighth paragraph beginning on page 8, with respect to the rejection of claims 1-4, 11-14, and 18-21 under 35 USC 102(b) as being anticipated by Conley, Applicant argues:

> "*The Examiner cites two different embodiments of Conley in alleged support of the rejection. (See Office Action, pages 3 and 4, #6b and page 19, #45). However, it is well settled that it is improper to combine features from different embodiments without requisite motivation.*"

40. The Examiner respectfully notes that the rejection presented supra is based on a single embodiment disclosed by Conley, the embodiment where the output of a modulo N counter is used as the value of field 43. Conley teaches at paragraph 0051 that the output of a module N counter is one way that field 43 may be written.

41. **Second point of Argument**

42. In the second paragraph beginning on page 9, with respect to the rejection of claims 1-4, 11-14, and 18-21 under 35 USC 102(b) as being anticipated by Conley, Applicant argues:

> "*Similarly to the time stamps, Conley necessarily needs to go through a step of comparing the counter values to one another to determine which page is the newest. To the contrary, a recited indicator immediately signals the status of the block. Accordingly, updating the counter value is not the same as or an equivalent of writing the "meta- information comprising flash memory state information comprising an indicator, which indicates a state of the physical block as valid, deleted, or invalid.*"

43. The Examiner respectfully notes that the claims as currently recited do not recite an indicator which immediately signals the status of the block. Claim 1 recites "*flash memory state information comprising an indicator which indicates a state of the physical block*".

44. **Third point of Argument**

45. In the third paragraph beginning on page 9, with respect to the rejection of claims 1-4, 11-14, and 18-21 under 35 USC 102(b) as being anticipated by Conley, Applicant argues:

> "*Additionally, the second cited embodiment of Conley likewise depends on time because the information about the page age is provided based on the number of counts which is increased each time the page is updated. Accordingly, the second cited portion of Conley does not teach or suggest providing "the flash memory state information which is time independent," as recited in claim 1.*"

46. The Examiner respectfully disagrees. The output of the modulo N counter for a second write will be one higher than the previous value stored for a first write to the logical block, whether the second write occurs one second, one day, or one year later than the first block. Accordingly, while the output of the modulo N counter is order dependent, it is time independent.

47. **Fourth point of Argument**

48. In the fourth paragraph beginning on page 9, with respect to the rejection of claims 1-4, 11-14, and 18-21 under 35 USC 102(b) as being anticipated by Conley, Applicant argues:

> "*Finally, the Examiner asserts that, when Conley erases the block, the time stamp field contains all 1s (see Office Action, page 4, lines 4-5. the Examiner further asserts that, when Conley erases the block, all the bits contained within that page are set to 1s. (See Office Action page 19, #45, lines 5-6). These*

statements are inconsistent with one another. Additionally, the Examiner does not provide any support in Conley for either of the statements. Therefore, it appears that the Examiner assumes that certain aspects of the invention exist in Conley, when they are, in fact, absent from Conley. Absent support for each and every element of claim 1 in Conley, the rejection is improper."

49. The Examiner respectfully submits that is unclear what Applicant is arguing is inconsistent between the statements that when a page is erased, the bits of field 43 (which is a part of the page, which is part of a block) are set to 1s, and when the block containing the page is erased the bits of the page are set to 1s. Both statements are stating that when the memory is erased, the bits are set to 1s.

50. With respect to Applicant's argument that Conley does not provide support for these statements, the Examiner notes that at paragraph 0047 Conley teaches that NAND flash is used. That when NAND flash memory is erased all the bits are set to 1s is inherent in the design of NAND flash, and is well known to one of ordinary skill in the art. The Examiner has included a reference (How Flash Memory Works) showing this.

Conclusion

51. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARED I. RUTZ whose telephone number is (571)272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christian Chace can be reached on (571)272-4190. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christian P. Chace/
Supervisory Patent Examiner, Art Unit 2187

Jared I Rutz
Examiner
Art Unit 2187

jir